Amendments to the Claims:

Claims 1-12 are currently pending in the application. Claim 1 is an independent claim, and claims 2-12 depend there from. Claim 1 is currently amended.

1. (Currently Amended) A system for reducing noise in a chip, the system comprising:

a substrate;

a first well disposed on top of said substrate;

a second well and a third well that are both disposed within said first well;

a first transistor disposed in said second well;

a positive potential of a quiet voltage source connected to a body of said first transistor; and

a second transistor disposed in said third well.

2. (Original) The system according to claim 1, wherein said first transistor is a PMOS transistor.

3. (Original) The system according to claim 1, wherein said second transistor is an NMOS transistor.

4. (Original) The system according to claim 1, further comprising a noisy voltage source coupled to a source of said first transistor.

5. (Original) The system according to claim 1, wherein a body of said first transistor is resistively coupled to said second well.

6. (Original) The system according to claim 1, further comprising a noisy voltage source, wherein a body and a source of said second transistor are both coupled to said noisy voltage source.

7. (Previously Presented) The system according to claim 1, wherein a body of said second transistor is capacitively coupled to said substrate.

8. (Original) The system according to claim 1, wherein said first well is a deep well.

9. (Original) The system according to claim 1, wherein said substrate is doped with a first dopant.

10. (Original) The system according to claim 1, wherein said first well is doped with a second dopant.

11. (Original) The system according to claim 1, wherein said second well is doped with a second dopant.

12. (Original) The system according to claim 1, wherein said third well is doped with a first dopant.